APPLICATION NOTE

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The behaviour of integrated bus hold circuits

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INTRODUCTION

The problem with floating or unused CMOS inputs as a general rule is that they must not be left floating otherwise due to gradual charging of the gate input capacitance, they may cause the following:

- There may be a static current flowing through the input stage, causing unnecessary excessive power dissipation.
- When the input voltage reaches the threshold level, the device may start high frequency oscillations causing heat generation that may eventually damage the part.

Therefore, as a standard solution, all unused (open or floating) inputs are simply connected to GND or V_{CC} to prevent these adverse effects.

In certain testing conditions, inputs may be left open, but certainly in bus applications, it may happen that inputs are effectively floating when all devices driving the bus are in 3-state. One should ensure that all inputs are defined “0” or “1” to prevent excessive heat dissipation or unwanted high frequency oscillations.

THE SOLUTIONS

The following are several solutions including their added costs, components counts, and effectiveness:

Static Pull-up/Pull-down Resistors

Static pull-up/pull-down resistors are a solution used very often to define the state of unused CMOS inputs when the bus is not driven by any device. Although these resistors cause additional power dissipation and increase component count, they are very effective. However, when using today’s narrow pitch packages such as TSSOP48-56, there may not even be enough space to add these pull-up/pull-down resistors on the PCB.

External Bus Hold Circuit

An external bus hold circuit (see Figure 1) is another solution which uses an inverter and resistor between its input and output. This circuit connects the input to GND or V_{CC} depending on the state of the input and holds the bus in this state, hence its name “bus hold”. Although this circuit reduces excessive power dissipation caused by static pull-up/pull-down resistors described earlier, it significantly adds to the component count and costs.

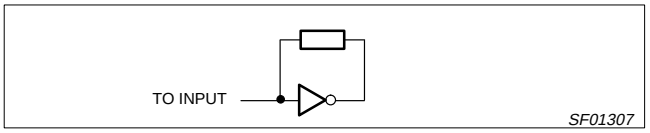

Figure 1. External Bus Hold Circuit

Integrated Bus Hold Circuit

Philips Semiconductors has applied integrated bus hold circuits (see Figure 2) for a number of logic families. Integrated bus hold circuits minimize additional power dissipation and provide additional component count internally at no extra cost for the device.

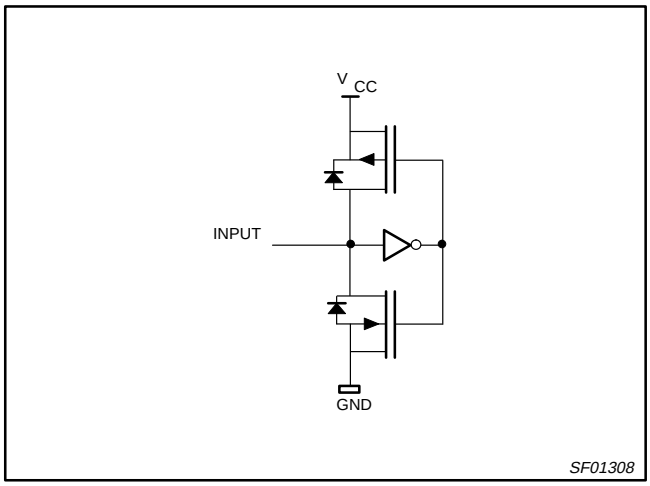

Figure 2. Integrated Bus Hold Circuit

The integrated Bus Hold circuit acts like dynamic pull-up/pull-down resistors as follows:

- When the input is at “0”, the output of the inverter is at “1” so that the lower FET is ON and acts like a pull-down resistor.
- Similarly, when the input is at “1”, the upper FET is activated and acts like a pull-up resistor.

When the input voltage varies, an input current will flow into or out of the input circuit (see Figure 3), so that when the input voltage rises, the input current will slowly increase, since the lower FET is conducting. Around the threshold level, the upper FET will then start conducting and the lower FET will stop conducting. Then the input current will reverse direction (input current flows out of the integrated bus hold circuit) slowly decreasing until the input voltage is at V_{CC}.

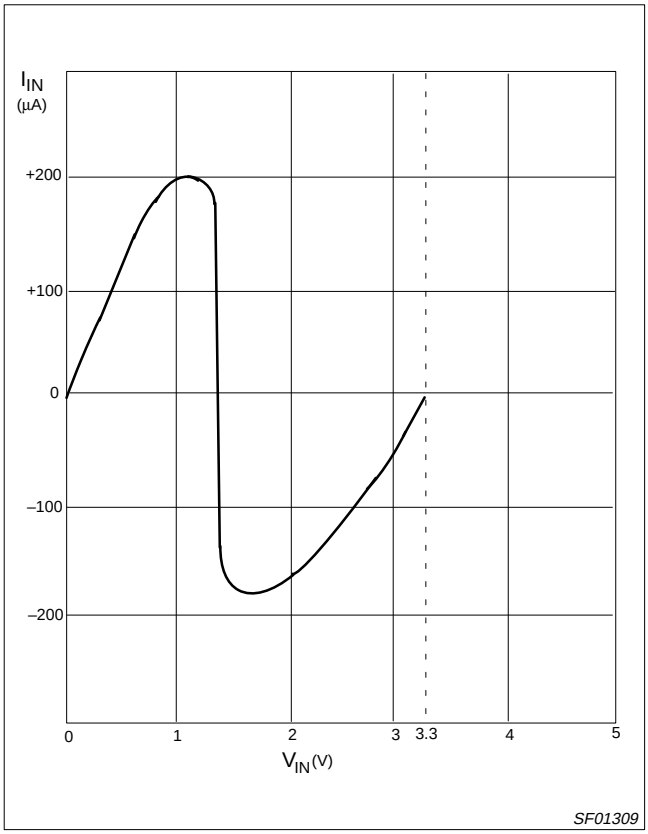

Figure 3. Input Voltage (V_{IN}) vs. Input Current (I_{IN})

Description

The following parameters describe the behaviour of the integrated bus hold circuit:

- IBHL (for LVT called I_{HOLD}) is the bus hold LOW sustaining current, that specifies an input current below which the bus hold circuit is keeping the input voltage lower than the 0.8V TTL switching level.
- Similarly, input current (IBHH), the bus hold HIGH sustaining current will yield an input voltage higher that 2.0V when the input is at “1”.
- IBHLO is the bus hold LOW overdrive current. When the input is driven with this current, the input will change from a “0” to a “1”.
- Similarly, IBHHO specifies the input current that will change the input from a “1” to a “0”.

INTEGRATED BUS HOLD CIRCUITS FOR 5V TOLERANT DEVICES

The circuit discussed in Figure 2 is the integrated bus hold circuit in its basic form as it is used in logic devices such as the ALVC.

However, logic transceiver functions that have 5V tolerant outputs also require the integrated bus hold circuits to be 5V tolerant. For such cases, the bus hold circuits have been provided with additional components to enable bus hold circuits to handle 5V operation.

Philips Semiconductors has provided two such solutions, the bus hold with Schottky diode and with dynamic backgate switching (see Figure 4) as follows:

Bus Hold with Schottky Diode

The standard solution for LVT devices uses a series Schottky diode (see Figure 4), which effectively blocks the current path from the input to V_{CC}.

Bus Hold with Dynamic Backgate Switching

The standard solution for LVCHXXXA devices is called dynamic backgate switching (see Figure 4), where the MOSFET is switched OFF when the input voltage exceeds V_{CC} and the current path through the diode is blocked by some switches.

Both bus hold circuits behave quite differently as shown in the V_{IN}/I_{IN} characteristics (see Figure 5) as follows:

- The input current for LVT (with Schottky diode) becomes zero when the input exceeds ($V_{CC} – V_{Fdiode}$).
- Whereas for LVCHXXXA devices with dynamic backgate switching have a hysteresis effect. When the input voltage exceeds (V_{CC} + 0.6V), the input FET is turned off, so the input current becomes zero. The upper FET is turned on again when the voltage becomes lower than (V_{CC} – 0.6V).

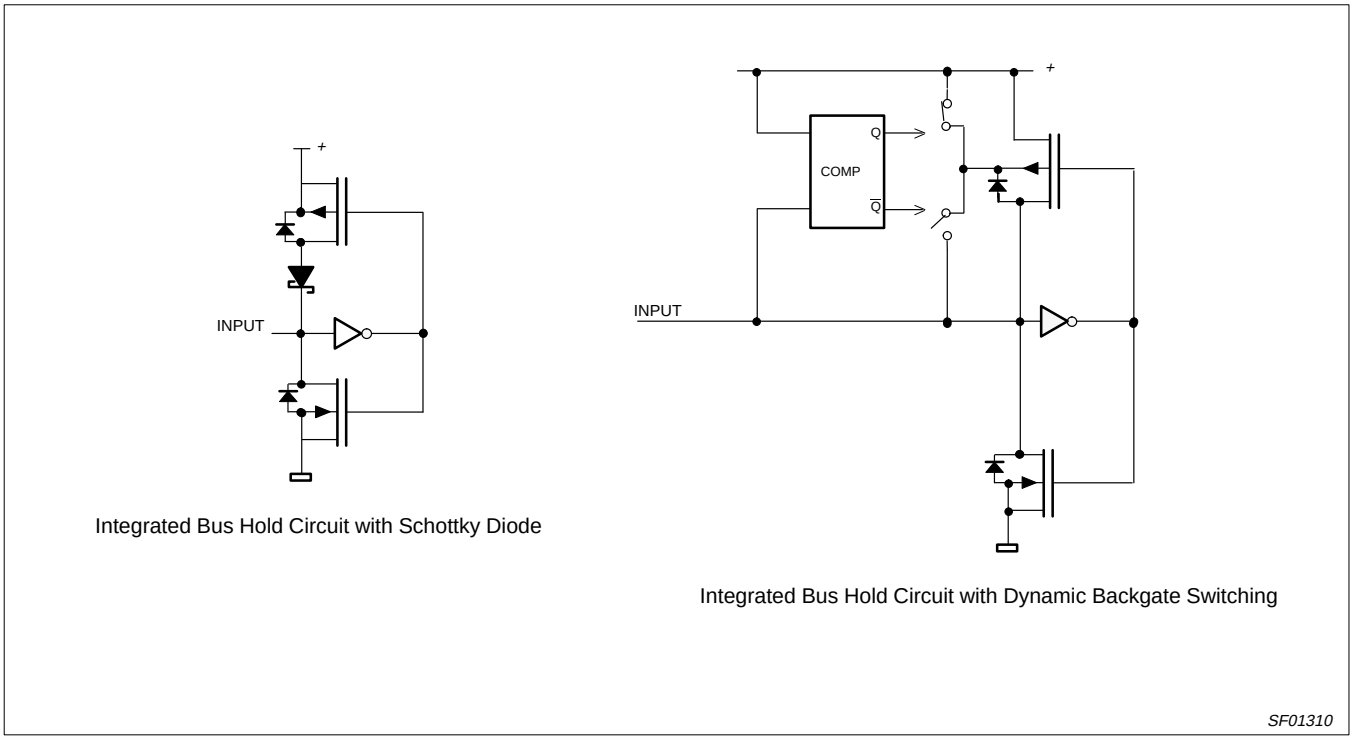

Figure 4. Integrated Bus Hold CIrcuits with Schottky Diode and Dynamic Backgate Switching

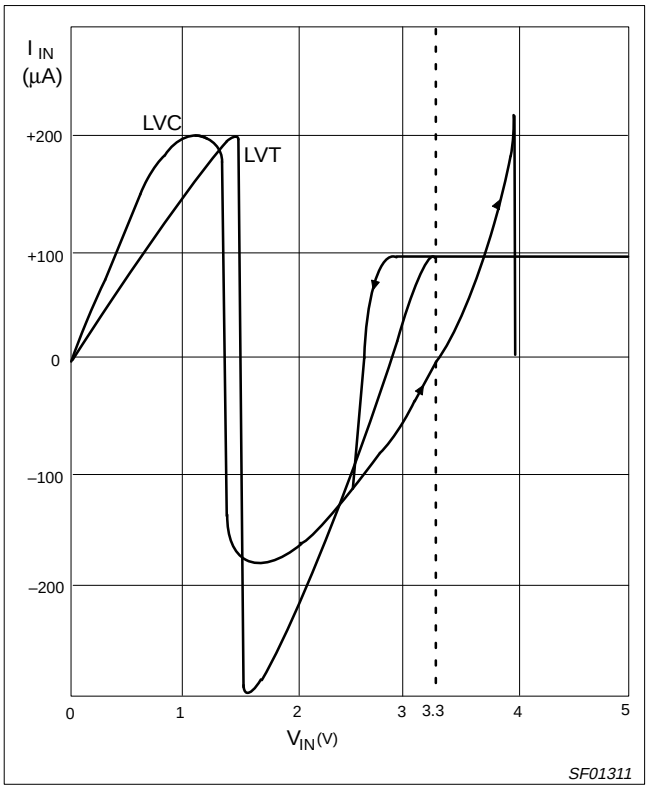

Figure 5. V_{IN} vs I_{IN} for 5V tolerant Integrated Bus Hold Circuits

DRIVING A BUS HOLD CIRCUIT

The input current is so low that virtually any part is capable of delivering enough current to toggle quite a number of paralleled inputs. At Philips Semiconductors we have performed tests with one (1) 74LV244 device (with 8mA output drive) driving from 0 to 10 74LVC244As (without integrated bus hold circuits) and compared them with 0 to 10 74LVCH244As (with integrated bus hold circuits). These tests showed that the effects of integrated bus hold circuits on the total propagation delay are negligible.

As a rule of thumb, adding one (1) integrated bus hold circuit gives an extra propagation delay of about 40 ps, so that one (1) LV device driving 10 integrated bus hold circuits will give an extra delay of 0.4ns. Families with a higher output drive will have a propagation delay that is proportionally shorter. For instance, one 74LVC244 (24mA driver) will have an extra propagation delay of about 15ps per integrated bus hold circuit load.

When applying parts with integrated bus hold circuits in backplane buses, where the total current flowing in the bus are so high, the desired effects of integrated bus hold circuits may be negligible. The current that an integrated bus hold circuit can handle is by far insufficient to pull an active bus high (“1”) or low (“0”). Only after all reflections are at a minimum can the integrated bus hold circuit become effective. Additionally, for crosstalk situations, the bus hold may be incapable of holding the bus to the required “1” or “0” state.

In some applications, the bus should become HIGH when all outputs driving the bus are in 3-state. In such cases, you should use a termination resistor, (R_T pulled-up to V_{CC}) which is low enough to overrule all the bus holds connected to that circuit. R_T is calculated as follows from equation 1:

EQUATION 1

$$R_T < \frac{V_{CC} - V_{TH}}{IBHHO}$$

where V_{TH} is the switching level HIGH
IBHHO is the maximum overdrive current; the typical value is about a factor of two lower

Example

With a V_{CC} of 5V, IBHHO = 500μA and TTL switching levels (i.e. V_{TH} = 2V), the termination resistor value should be less than 6kΩ. Therefore, when more inputs are connected to the bus, this value is proportionally lower.

Power Dissipation Effects

Since a bus hold effectively forms a pull-up or pull-down resistor, it will dissipate extra power when the input changes state. Additionally, the driver must deliver extra current which creates more dissipation in the driver.

Using conservative assumptions, you can calculate the following parameters from equation 2 for low voltage families when $2.7V < V_{CC} < 3.6V$:

EQUATION 2

$$P_{BH} \leq f \times T_T \times \frac{I_{HOLD} \times V_{CC}}{2}$$

where P_{BH} is the dissipation in the bus hold circuit itself
T_T is the average of the rise and fall times of the input signal
f is the frequency of the input signal

One important consequence of the above equation is that the dissipation of bus hold is dependent on the input rise and fall times which are primarily determined by the output drive capability of the driving component and the capacitive load.

The frequency, f in the equation is normally NOT equal to the clock frequency, it is an effective input frequency. For example, if the input is HIGH for a long time, the dissipation during that time is essentially zero. Therefore, you should estimate the number of transitions based on a practical occurrence of “0’s” and “1’s”.

From equation 2, if IBHHO = 500μA and V_{CC} = 3.3V, the following worst case dissipation value in μW can be determined from equation 3 as follows:

EQUATION 3

$$P_{BH} \leq f \times T_T$$

where f is in MHz and
T_T is in ns

Typically, the power dissipation is about half the value of P_{BH}.

Family Survey and Nomenclature

Philips Semiconductors has integrated bus hold circuits in some advanced BiCMOS and CMOS families which are identified by the letter “H” in its the part number (the exceptions are LVT and LVT16 families) as follows:

- A standard bus hold circuit with current path to V_{CC} is built in the following:
  - **LVCH** and **ALVCH**
- An enhanced bus hold circuit without current path to V_{CC} is built in the following:
  - **LVT**, **LVT16**, **ABTH**, and **ABTH16** using a Schottky diode arrangement
  - The 5 Volt tolerant **LVCXXXA** devices that use dynamic backgate switching.
- Families such as **LV**, **LVC**, **HLL**, **ABT**, **ABT16**, and all **5V CMOS** have no bus hold circuits.

Conclusion

This application note discusses the effects of bus hold circuits as applied by Philips Semiconductors in their advanced CMOS and BiCMOS logic families. Logic devices with bus hold circuits can have floating (open) inputs without any negative effects. They have a low power dissipation compared with using static pull-up or pull-down resistors and most importantly because they are integrated, they do not increase component count, keep costs low, and optimize the available space on the PCB.

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